IN THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please **AMEND** the claims according to the following

Please **CANCEL** claims 14, 16 and 18.

1. (CANCELLED)

2. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, wherein said specific application-purpose instruction operating unit is built in as an intellectual property of an ASIC (Application Specific Integrated Circuit).

3. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, wherein the number of cycles control to issue the same succeeding instructions.

4. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, further comprising:

a rewritable register provided within a processor core of the processing apparatus, wherein

said rewritable register prescribes a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to use a result thereof, and said issuing of the instruction is controlled based on said number of cycles.

5. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, further comprising:

a rewritable register provided within a processor core of the processing apparatus, wherein

said rewritable register prescribes a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is the same as the instruction of said specific application-purpose instruction operation unit, and said issuing of the same instruction in succession is controlled based on said number of cycles.

6. (PREVIOUSLY PRESENTED) An information processing apparatus, comprising:

a control unit to process an operation instruction, which does not have a functional specification, as a specific application-purpose operation instruction;

a specific application-purpose instruction operating unit to support a flexible pipeline structure and to carry out an operation of the specific application-purpose operation instruction for each application field;

a rewritable register to prescribe a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is same as the instruction of said specific application-purpose instruction operation unit, wherein the instruction of said specific application-purpose instruction operating unit occupies an operating unit source; and

a flag provided within a processor core of the processing apparatus,

wherein said flag changes over between a case where a number of cycles, which is prescribed from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue the same instruction in succession, becomes the same as another number of cycles, which is prescribed from when the instruction of the specific application-purpose instruction operating unit is issued to when it becomes possible to use a result thereof, and a case where it is possible to issue the same instruction in succession in each cycle, and said issuing of the instructions is controlled based on the flag.

7-12 (CANCELLED)

13. (PREVIOUSLY PRESENTED) The exception processing method according to claim 15, further comprising:

determining before the execution of the execution processing, whether to perform the exception processing by checking whether the second instruction causing the interruption is a

specific application-purpose operation instruction.

14. (CANCELLED)

15. (CURRENTLY AMENDED) ~~The~~An exception processing method ~~according to claim 14, further~~ for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of interrupt processing, exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction, the exception processing method comprising:

setting, when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception in a register or a flag;

determining when the interruption is caused by the second instruction, whether the exception has occurred by reading the register or the flag;

performing the exception processing for the first instruction, if the exception has occurred according to the reading of the register or the flag;

performing the interrupt processing for the second instruction to return from the interruption; and

determining before the execution of the exception processing, whether to perform the exception processing by reading a second register or a second flag that stores an operation mode indicating to the processor whether to perform the exception processing.

16. (CANCELLED)

17. (CURRENTLY AMENDED) ~~The~~An exception processing method ~~according to claim 14, further~~for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of interrupt processing, exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction, the exception processing method comprising:

setting, when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception in a register or a flag;

determining when the interruption is caused by the second instruction, whether the

exception has occurred by reading the register or the flag;

performing the exception processing for the first instruction, if the exception has occurred according to the reading of the register or the flag;

performing the interrupt processing for the second instruction to return from the interruption; and

determining before the execution of the exception processing, whether to perform the exception processing by checking whether a value, which is stored in a second register or a second flag and is associated with the second instruction that has caused the interruption, indicates the processor to perform the exception processing.

18. (CANCELLED)

19. (CANCELLED)

20. (PREVIOUSLY PRESENTED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when the operation exception has been detected during the execution of the specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during the execution of a trap instruction to generate the interruption,

wherein

said interruption control unit carries out a control relating to the generation of an interruption, when said interruption control unit has received a notice that the interruption is generated, and

when said flag control unit has received an operation exception detection flag invalidate instruction, said flag control unit invalidates said operation exception detection flag.

21. (PREVIOUSLY PRESENTED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when the operation exception has been detected during the execution of the specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during the execution of a trap instruction to generate the interruption,

wherein said interruption control unit carries out a control relating to the generation of an interruption, when said interruption control unit has received a notice that the interruption is generated, and when said flag control unit has received an operation exception detection flag read instruction, said flag control unit reads the value of said operation exception detection flag.

22. (PREVIOUSLY PRESENTED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when the operation exception has been detected during the execution of the specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during the execution of a trap instruction to generate the interruption,

wherein said interruption control unit carries out a control relating to the generation of an interruption, when said interruption control unit has received a notice that the interruption is generated, and when said flag control unit has received an operation exception detection flag write instruction, said flag control unit writes a value into said operation exception detection flag.

23. CANCELLED

24. (PREVIOUSLY PRESENTED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a condition code register that is set based on a value that is held in said operation exception detection flag;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when the operation exception has been detected during an execution of the specific application-purpose operation instruction;

a flag control unit setting the condition code register based on a value that is held in said operation exception detection flag; and

a branch/interruption return instruction control unit determining whether an interruption is generated or not based on a value held in said condition code register and a value shown by an instruction field during the execution of a trap instruction to generate the interruption, and, when the interruption is to be generated, notifying an interruption control unit that the interruption due to the operation exception of a specific application-purpose operation instruction is to be generated,

wherein said interruption control unit carries out a control relating to the generation of an interruption, when said interruption control unit has received a notice that the interruption is generated.

25. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag invalidate instruction, said flag control unit invalidates said operation exception detection flag.

26. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag read

instruction, said flag control unit reads the value of said operation exception detection flag.

27. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag write instruction, said flag control unit writes the value into said operation exception detection flag.

28. (ORIGINAL) The information processing apparatus according to claim 24, wherein

said information processing apparatus has an instruction having an operational function specialized for an image processing as the specific application-purpose operation instruction.

29-32 (CANCELLED)